

Low-latency HDR Tonemapping

Hardware accelerator for tonemapping HDR video on an FPGA

Diplomand



Remo Schraner

Einleitung: The dynamic resolution of displays and image formats is traditionally limited to 8bit per color channel. This is nowhere near enough to capture most real-world scenarios at a linear scale. To compress the source information into the available range, a tonemapping operator is applied, which exploits the non-linearity of the human perception by resolving darker areas with a higher percentage of the output range. This is usually done with logarithmic functions.

The goal of this thesis was to implement a hardware accelerator for such a tonemapping operator that can augment FPGA based computer vision applications. While software solutions exist, they require a graphics processor for video streaming. This comes at a notable power draw and latency, making it unsuitable for embedded applications with real-time constraints.

Vorgehen: To achieve a small hardware footprint and a low latency, the algorithm according to F. Drago et al. was chosen. It approximates the human perception with a logarithmic function of a base that varies relative to the pixel brightness.

The existing C++ implementation available from openCV was adapted and implemented as a dedicated hardware circuit in VHDL. The proposed implementation operates on a pixel-based stream: As this is a global tonemapping operator, it applies the same ("global") function to each pixel separately. There is no dependency on the local neighborhood, leading to a low computational complexity and making a line or frame buffer superfluous.

Ergebnis: This work enables existing hardware accelerated image processing applications to interface with sources of a higher dynamic range than they natively would support. The design achieves up to 200Mpx/s throughput on an AMD Ultrascale+

architecture and requires roughly 5% of the hardware available on a medium-sized FPGA. At a latency below 1us and a dynamic power draw of 0.26W it is well suited for applications with constraints that would prohibit the deployment of a "general purpose" graphics processor.

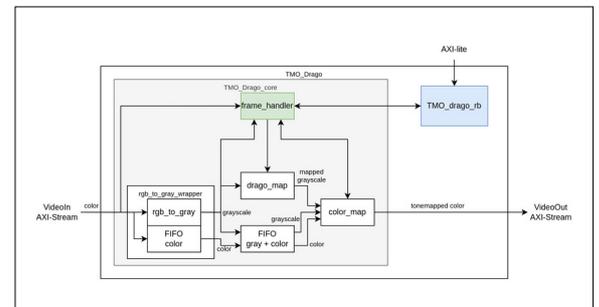
Algorithm: bias, sat and gamma are user parameters. GA is a dynamic adaption factor from the previous frame.
Eigene Darstellung

$$L = 0.299 \cdot R + 0.587 \cdot G + 0.114 \cdot B$$

$$L_c = \frac{\log_2(1 + L \cdot GA)}{\log_2(2 + 8 \cdot L^{\ln(\text{bias})/\ln(0.5)})}$$

$$\{R', G', B'\} = \left(\frac{\{R, G, B\}}{L} \right)^{\text{sat}/\gamma} \cdot L_c^{1/\gamma}$$

Blockdiagram: RGB image is converted to grayscale (luminance) and tonemapped. Then, color is restored.
Eigene Darstellung



Concept: Information from lower, mid and upper bit values of 14bit source (left) are compressed into an 8bit range.
original HDR source: <https://www.pdfrehner.ch/>



Referent

Prof. Dr. Paul Zbinden

Korreferent

Dr. Peter Schwider,
Photonfocus, 8853
Lachen, Schwyz

Themengebiet

Electrical Engineering